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S-Hybrid Step-Down DC–DC Converter—Analysis of Operation and Design Considerations

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S-Hybrid Step-Down DC-DC Converter—Analysis of Operation and Design Considerations

***Abstract*—The paper presents a new highly-integrable hybrid step-down converter that merges switched-inductor (SI) and switched-capacitor (SC) operations and significantly reduces on-board loss by using input cable's parasitic inductance as its main inductor. This converter has the inductor placed at the input with a smaller voltage swing leading to possible utilization of smaller inductor and low voltage rating switches that generally translates to lower conduction loss. Analyses of converter operation and losses to reveal its original characteristics and design guidelines are presented to facilitate the components optimization. The converter architecture is verified by a proof-of-concept 15-W inductor-less Li-ion battery charger prototype that utilizes a 1 m USB 3.0 cable as inductor. The converter, switched at 2 MHz from a 5 V input, experimentally achieves 89.7% peak efficiency and 6.0% higher efficiency at full load than a Buck converter counterpart. High efficiency and zero on-board inductor yield a relative 45.7% on-board loss reduction at full load, promising excellent integration feasibility and superior system thermal management.**

***Index Terms*—Buck converter, DC-DC, inductor-less power converter, S-Hybrid converter, step-down power conversion, smart power cable.**

I. INTRODUCTION

MOBILE devices such as smartphones have become ubiquitous while their system complexity has steadily increased for more functionalities in limited space. Since they are all battery-powered, they need to have regulators that charge battery and supply power to a variety of blocks, i.e. processors, with high efficiency in both power conversion and space utilization [1]. Low drop-out (LDO) regulator has conventionally been the default option for mobile battery charger because of its simplicity and compact size. However, it is no longer satisfactory due to its poor efficiency that causes critical thermal issues when desirable power/current capacity for battery chargers increases.

For efficient power conversion, switched mode power supplies including switched-inductor (SI) and switched-capacitor (SC) converters have been actively engineered to replace LDOs [1], [2]. In general, SI converter that transfers charge in form of current features fine regulation and high efficiency across a wide range of input and load variations. However, the reliance on inductor in this type of converter are undesirable for miniaturization and integration [2]. In conventional SI converters, high inductance is required for tight regulation and low output ripple, but its equivalent series resistance (ESR) that is often proportional to the inductance can significantly degrade the efficiency especially in mobile applications with space limitations. To reduce the ESR, inductor often needs to be large and bulky. For instance, Buck converter is a representative of SI converter for a voltage step-down function. In order to reduce output voltage ripple from a large switching-node voltage swing at the inductor, Buck converter uses a large inductor [3]. In addition, because of its configuration, the Buck's inductor is forced to carry the full output current, making inductor copper loss become one of the major power losses in this architecture.

Three-level Buck converter employs a switched capacitor at the input to half voltage swing across an output inductor in order to reduce inductance and thus features better integration [4]. Reduced voltage swing together with interleaving effect enables significant reduction of inductor current ripple and inductor size. On the other hand, the three-level circuit construction doubles the number of switches, i.e. at least from one to two active switches with diodes or from two to four switches with synchronous implementation, leading to a more complex control circuitry. In addition, the inductor is still placed at the output and exposed to the same output current and associated loss with a Buck converter counterpart that, in turn, sets a miniaturization limit [3].

As an alternative to the SI converters, SC converters utilizing capacitors for power conversion show better miniaturization because no bulky inductor is involved and on-chip capacitors are readily available [5], [6], [7]. As a key drawback for this type of converter, SC converters can only achieve high efficiency when its output voltage is close to predetermined fractions of input voltage, e.g. 1/2, 1/3, 2/3. To achieve fine regulation in between these conversion ratios, for example when input voltage and/or output voltage varies, it must sacrifice efficiency or require additional techniques and/or

circuitry to maintain efficiency [8].

To overcome the drawbacks and to exploit advantages from both inductor and capacitor, recent works [9], [10], [11] show emerging efforts in combining both passive elements in hybrid structures. The remaining problems are (a) they still require explicit inductors that are hard to miniaturize and (b) their circuit complexity degrades efficiency and limits applications.

This paper discusses a new hybrid power conversion architecture that eliminates dedicated inductor in the circuit by utilizing parasitic inductance available in the system. As a promising example, a USB cable, commonly used to connect a mobile device to an input source such as a computer or adapter, has significant inductance, ranging from hundreds nanohenries to several microhenries dependent on its length, materials, and manufacturer [12]. This cable inductance is often ignored, or engineering efforts are put in designing filters, e.g. adding decoupling capacitors at its ends, to remove its effect. It was recognized that this parasitic inductance can be utilized to provide power conversion to improve the system efficiency and heat distribution. To realize utilization of parasitic inductance on input USB cable for power conversion, a new converter named *S-Hybrid* was proposed in [12]. The new power delivery architecture employing S-Hybrid converter can eliminate explicit inductors required in other SI converters, enabling the cable to be used for both power transmission and power conversion. Without unnecessary magnetic component and associated loss, the converter can achieve higher mid-to-heavy load efficiency which is critical in mobile applications since it defines power delivery limitation.

With a unique combination of SI and SC operations, the converter features original characteristics different from conventional SI or SC converters, for example trade-offs between 1) capacitor size ratios and output voltage ripples and 2) duty cycle-dependent non-linear loss contribution of switches. In this paper, we provide extended analyses of converter operation and design guidelines to help optimize the converter performance for a better design. The paper therefore is organized as follows. Section II first reviews the topology and circuit operation. Steady state analysis of S-Hybrid converter compared to Buck-type converters is presented in Section III to reveal the original features of the architecture. Section IV provides design analysis and guidelines for capacitors and semiconductor switches. Measurement results from a 15-W prototype converter verifying the converter architecture and predicted performance are presented in Section V, and the paper is finally concluded in Section VI.

II. S-Hybrid Converter

To better understand the converter architecture, this section provides a background of cable impedance usage and review of S-Hybrid converter.

A. Utilization of Cable as Inductor

In order to utilize a cable as an inductor, analysis on the cable parasitics is required. A transmission line model with lumped elements can be used to represent parasitic impedances of a two wire cable (see [13] for more details). The cable inductance is

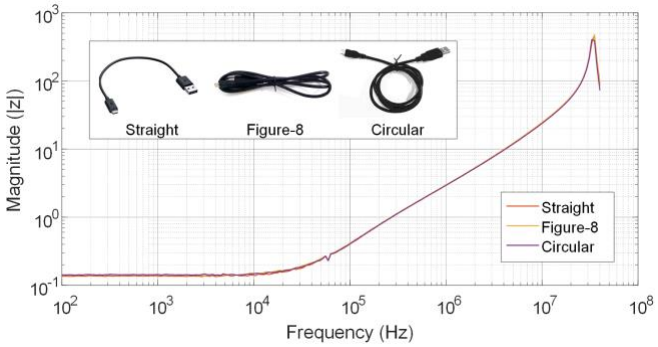


Fig. 1. Impedance measurements of a USB 3.0 cable with different shapes.

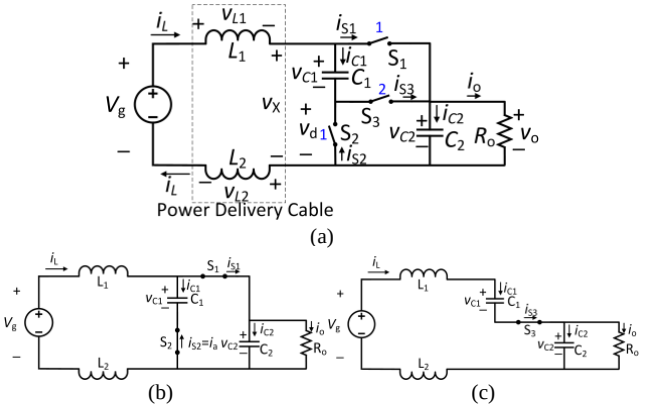


Fig. 2. S-Hybrid step-down converter: (a) converter schematic, (b) subcircuit in phase 1, (c) subcircuit in phase 2. The hybrid converter utilizes input cable as inductor for power conversion eliminating the need for dedicated inductor while merging SI and SC operation to retain the circuit simplicity.

significant while the effect of equivalent shunt capacitance is negligible up to ~10 MHz in practical USB cables [12]. Fig. 1 displays three impedance measurements of a USB cable used in this paper in three different shapes, showing no significant difference between them. In other words, the impedance and thus the inductance of the cable are independent of its shape. This is because the ground shield of the cable encloses the signal and power wires and keeps the field inside the USB cable and independent of the outside environment.

The inductance of the cable, however, depends on the length and physical layer construction of the cable, as described in [12]. Since the focus of this paper is on analysis of the converter operation to reveal its original topological characteristics to help optimize the performance, we assume a certain range of cables that provide an inductance large enough for the required power conversion. More details on converter control with different cables will be provided in Section IV.

B. S-Hybrid Converter Topology

Enabling a converter to use less inductance, and thus smaller inductor and system size, is key to miniaturization and possibly better integration. The S-Hybrid converter topology was created along these aims at inductance reduction and optimal position of inductor in the topology while utilizing cable parasitics for power conversion.

The schematic of S-Hybrid step-down DC-DC converter is shown in Fig. 2(a). In series with input inductors L_1 and L_2, the

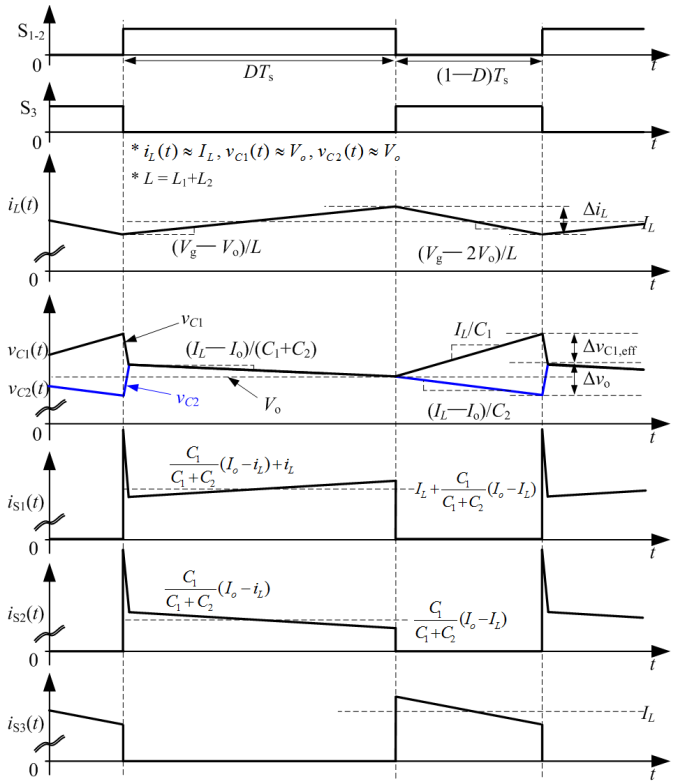


Fig. 3 Circuit operation of S-Hybrid converter. The operational waveforms illustrate combination of SI and SC operations where inductor is balanced by two voltage domains and the capacitors are balanced by the SC network.

network of switches $S_{1\text{-}3}$ and capacitors $C_{1,2}$ is operated to: 1) switch the "spring" potential v_x to regulate the output with an inductor similar to an SI converter, and 2) transfer and balance the charge from C_1 to C_2 similar to an SC converter. Ideally, voltages across C_1 and C_2 are equalized every switching cycle. Operations of C_1 and C_2 allow the inductors to only block V_{C1} that is equal to V_o and smaller than input voltage V_g.

C. Circuit Operation of S-Hybrid Converter

To explore main features of S-Hybrid converter, its circuit operation is discussed in this subsection. For simplicity in the following analysis, we assume ideal switches for $S_{1\text{-}3}$ and small ripple approximation for inductor current i_L and capacitor voltages v_{C1} and v_{C2} [14].

The converter is operated in two phases as depicted in Fig. 2 and Fig. 3. Phase 1 starts when S_1 and S_2 are turned on shorting C_1 to C_2. L_1 and L_2 start to be charged by $(V_g - V_o)$. After a short charge transfer from C_1 to C_2 equalizing v_{C1} and v_{C2} to V_o, the two capacitors supply the output together with inductor current. The current distribution between capacitors is determined by their ratio as noted in Fig. 3. In phase 2, S_1 and S_2 are turned off while S_3 is turned on, charging v_x to $2V_o$, defined by the series connection of C_1 and C_2 via S_3. Since $2V_o$ is larger than V_g, the inductor current discharges in this phase with the slope of $(V_g - 2V_o)/L$. During phase 2, the load is supported by C_2 and the charge from the inductor current that also charges C_1 in series. It is important to note that the L_1 (L_2) is directly connected to C_1 (C_2) and switching operation of L_1 and L_2 are merged into that of C_1, minimizing the number of switches and associated loss.

TABLE I. COMPARISON OF INDUCTOR CURRENT RIPPLES

	Δi_L as a function of D	Δi_L as a function of M
S-Hybrid, $\Delta i_{L,\mathrm{S-Hybrid}}$	$\frac{V_g D(1-D)T_s}{L(2-D)}$	$\frac{(1-M)(2M-1)}{M}\frac{V_g T_s}{L}$
Buck, $\Delta i_{L,\mathrm{Buck}}$	$\frac{V_g D(1-D)T_s}{L}$	$M(1-M)\frac{V_g T_s}{L}$
Three-level Buck, $\Delta i_{L,\mathrm{3L-Buck}}$	$\frac{V_g\left(D-\frac{1}{2}\right)(1-D)T_s}{L}$	$\left(M-\frac{1}{2}\right)(1-M)\frac{V_g T_s}{L}$

*Equations for three-level buck converter are only valid for D≥0.5.

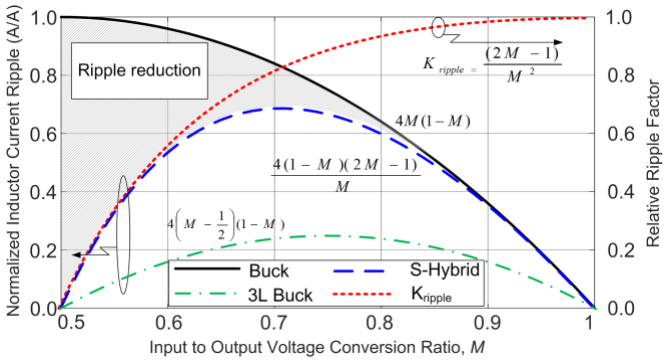


Fig. 4. Comparison of S-Hybrid converter's inductor current ripple to Buck type converters. Note that the relative ripple ratio is a function of M giving more advantages to S-Hybrid in smaller M while three-level buck converter achieves smallest ripple across the range.

With the circuit operation detailed above, the converter's ideal conversion ratio is derived by volt-second balance of inductor as

$$M = \frac{V_o}{V_g} = \frac{1}{(2-D)} \quad (1)$$

where D is the duty ratio of switch S_1 and S_2 as illustrated in Fig. 3. In this configuration, M ranges from 0.5 to 1.

III. STEADY STATE ANALYSIS OF S-HYBRID CONVERTER

In order to reveal the original features of S-Hybrid converter from the new hybrid configuration, this section analyzes its steady-state operation compared to Buck and three-level Buck converter counterparts.

A. Reduction of Inductor Requirement

Better inductance utilization and reduction of inductor requirements are key advantages of the hybrid topology that can be explained in terms of inductor loss. Inductor loss, one of the major losses in a step-down converter [10], includes DC loss caused by inductor DC resistance and current, and AC loss by its AC resistance and current ripple. While in a normal Buck or a three-level Buck converter the inductor is at output and handles full load current, S-Hybrid architecture's inductor is organized at the input and handles only input current, which is a fraction of output current. Therefore, a comparison using the same inductor, i.e. same ESR, would give the S-Hybrid architecture a factor of M^2 lower in DC loss. More discussion can be found in [12].

To achieve smaller inductor AC loss, small inductor ripple is required. Small inductor ripple translates to less reliance on inductor because it enables inductor size reduction that leads to better miniaturization with higher efficiency. Table I lists

fundamental relations between the inductor current ripple and other circuit parameters: input voltage V_g, inductance L, duty cycle D, and switching period T_s in S-Hybrid, Buck, and three-level Buck converters.

Given the same circuit parameters, the three converter types are compared in terms of inductor current ripple figures to evaluate their reliance on inductor. Since the same duty cycle D does not translate to the same conversion ratio, we can use the equations with conversion ratio M for the ripple comparison. In Fig. 4, these inductor current ripples are normalized by $(V_g T_s/4L)$ and plotted in the same x-axis. S-Hybrid converter achieves lower inductor current ripple than Buck converter across the operating range of conversion ratios. The amount of ripple reduction increases toward lower conversion ratios where the inductor voltage swing is gradually reduced while, in Buck converter, it stays constant at the input voltage. The relative ripple ratio K_{ripple} is defined as

$$K_{ripple} = \frac{\Delta i_{L,\text{S-Hybrid}}}{\Delta i_{L,\text{Buck}}} = \frac{(2M-1)}{M^2}. \quad (2)$$

On the other hand, compared to S-Hybrid converter, three-level Buck converter shows lower overall inductor current ripple mainly because of its interleaving operation by nature [15]. It should also be noted that the three-level configuration increases circuit complexity and its inductor still experiences output current, resulting in M^2 higher inductor DC loss and difficulty in miniaturization.

S-Hybrid topology exploits the benefit of a hybrid topology in reducing inductor current ripple, thus inductance reliance and AC loss similar to three-level Buck converter and strategizes a better inductor location to reduce its DC loss. To further analyze its characteristics, the following section will provide an average model of losses that will lead to S-Hybrid converter design insights and parameter optimizations.

B. Average Model of S-Hybrid Converter

To derive the average model of S-Hybrid converter, resistances of inductor and switches are added to the original schematic as shown in Fig. 5(a). We also assume small ripples for inductor and switch current and capacitor voltages. With the steady state operation in continuous conduction mode (CCM) assumed, inductor volt-second balance and capacitor charge-second balance are used to derive a new input to output voltage conversion ratio to incorporate the primary loss factors. By averaging the state equations from Fig. 5(b) and Fig. 5(c), averaged equations for L, C_1, and C_2 are derived as

$$\langle v_L \rangle = V_g - I_L R_L - V_{C2} - D' I_L R_{S3} - D' V_{C1} - D I_x R_{S1} \quad (3)$$

$$\langle i_{C1} \rangle = I_L - D I_x \quad (4)$$

$$\langle i_{C2} \rangle = D I_x + D' I_L - \frac{V_{C2}}{R_o} \quad (5)$$

where $D' = (1-D)$ and I_x is defined as average value of i_{S1} during DT_s. And we identify that $\langle v_L \rangle = \langle i_{C1} \rangle = \langle i_{C2} \rangle = 0$ in steady state. Combining (4) and (5), one can find

$$(2-D) I_L = \frac{V_{C2}}{R_o} = I_o \quad (6)$$

which is the same with the ideal condition analysis in Section II. To eliminate V_{C1} in (3), the relationship between V_{C1} and V_{C2} for voltage equality in Fig. 5(b) is used as

$$I_x R_{S1} + V_{C2} = -(I_x - I_L) R_{S2} + V_{C1}. \quad (7)$$

Eliminating I_L and I_x in (7) using (6) yields

$$V_{C1} = V_{C2} + \frac{V_{C2}(R_{S1} + D' R_{S2})}{R_o D (2-D)}. \quad (8)$$

Using (6) and (8), elimination of I_L and V_{C1} in (3) and solution for V_{C2} yields the effective input-to-output voltage conversion ratio M_{eff} accommodating the parasitic components,

$$M_{eff} = \frac{V_{C2}}{V_g} = \frac{1}{(2-D)} \frac{1}{1 + \frac{R_L + \frac{R_{S1}}{D} + \frac{D'^2 R_{S2}}{D} + D' R_{S3}}{(2-D)^2 R_o}}. \quad (9)$$

The effective converter conversion ratio reflects the effect of resistive components which is plotted in Fig. 6.

As noted in (9), each resistance component has different impact on the converter performance. To better analyze their effects and compare to other converters, equivalent circuit model is constructed. Reorganizing the right side of (9) lead to

$$M_{eff} = \frac{1}{(2-D)} \frac{R_o}{R_o + \frac{R_L + \frac{R_{S1}}{D} + \frac{D'^2 R_{S2}}{D} + D' R_{S3}}{(2-D)^2}} \quad (10)$$

which can be equivalently expressed by a general equivalent circuit model in Fig. 7 with an ideal DC transformer with turns ratio 1:M=1/(2—D) and output impedance R_{out} expressed as

$$R_{out} = \frac{\left(R_L + \frac{R_{S1}}{D} + \frac{D'^2 R_{S2}}{D} + D' R_{S3}\right)}{(2-D)^2}. \quad (11)$$

Using the equivalent circuit model, one can predict the

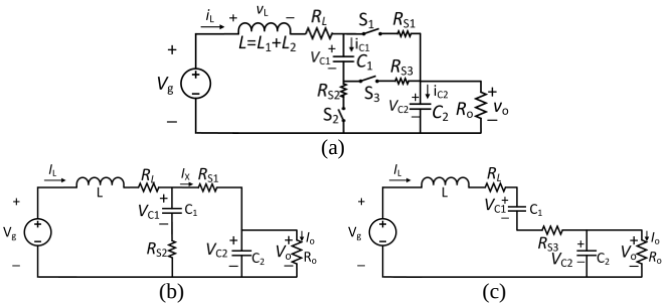


Fig. 5. Schematic to include non-ideal components: (a) converter circuit, (b) equivalent circuit for phase 1, (c) circuit for phase 2.

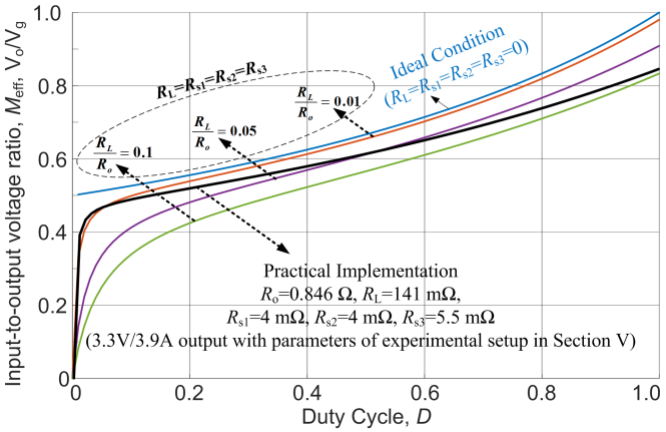


Fig. 6. Effective input-to-output voltage conversion ratio M_{eff} with different resistive components.

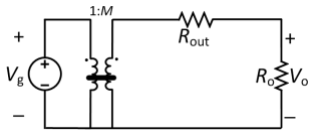


Fig. 7. Average model of a converter to represent major loss components.

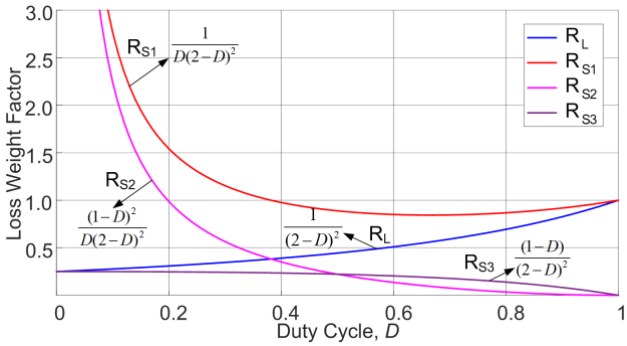


Fig. 8. Loss weight factor comparison. Using the factors, different impacts of switch on-resistance in different operating condition can be investigated.

converter performance such as efficiency or loss and utilize it to design circuit components.

To provide more insight from the average model, Fig. 8 displays weight factors comparison of the four loss components in S-Hybrid converter output impedance. Loss weight factor of R_i is found by normalizing its conduction loss to $I_o^2 R_i$ while input voltage and duty cycle D are varied but output voltage and load R_o are kept constant. This loss weight factor analysis that illustrates a trend when each loss could become critical can be used for switch optimization with more details in Section IV. For example, as D decreases, input current decreases and so does the inductor copper loss associated with R_L. When D decreases below 0.5, S_1 and S_2 conduction losses increase quickly because significantly increased charge in capacitor C_1 during phase 2 needs to be transferred to C_2 during phase 1 via S_1 and S_2.

The same average model analysis is employed to calculate M and R_{out} of Buck and three-level Buck converters to compare against S-Hybrid converter in Table II. To compare them at same operating conditions, duty cycle is converted to conversion ratio M in expressions of R_{out}. In case of Buck-type converters, R_{S1} and R_{S4} denotes the on-resistances of active switches and R_{S2} and R_{S3} denote the on-resistances of synchronous switches. As noted in Table II, while Buck and three-level Buck converter have conduction loss in a linear function of M and D, the S-Hybrid topology has non-linear loss increase clearly observed at low duty cycles that results from hard switched-capacitor actions in phase 1. This could be allieviated by a method of soft-switching technicques as described in [16], [17] which is beyond the focus of this paper. On the other hand, together with a factor of M^2 reduction (M<1) in inductor copper loss, advances in semiconductor technology, e.g. wideband gap devices such as GaN, which overcomes regular MOSFET limits, can expand a wide range of applications for this proposed architechture.

TABLE II. EQUIVALENT CIRCUIT PARAMETERS OF THREE CONVERTERS.

	M	DC Output Impedance, R_{out}
S-Hybrid	1/(2—D)	$M^2R_L + \frac{M^3}{(2M-1)}R_{S1} + \frac{M(1-M)^2}{(2M-1)}R_{S2} + M(1-M)R_{S3}$
Buck	D	$R_L + MR_{S1} + (1-M)R_{S2}$
Three-level	D	$R_L + M(R_{S1}+R_{S4}) + (1-M)(R_{S2}+R_{S3})$

IV. DESIGN CONSIDERATIONS

This section provides design considerations for S-Hybrid converter realization. While designing an inductor is a key in conventional power regulator design, this S-Hybrid converter can be designed to support an inductor given from a range of input cables. Depending on inductance and switching frequency, the converter can operate more in CCM or in discontinuous conduction mode (DCM). Once parasitic inductance of the input cable is provided, a switching frequency is determined to ensure that inductor current ripple is limited to prevent excessive inductor copper loss, e.g. <20% of average inductor current at rated load condition. Therefore, this section focuses on the considerations for capacitors and semiconductor switches.

A. Capacitor Design

Capacitor design considerations are twofold: 1) to identify optimal capacitance ratio C_2/C_1 to minimize the switched-capacitor loss and 2) to determine capacitance values to meet the system requirement such as output voltage ripple and space limit.

An optimum C_2/C_1 ratio can be determined by considering capacitor voltage ripples and switched-capacitor loss [6] that occurs when the converter transients from phase 2 to 1. The voltage ripple on C_2 is required to meet an output ripple constraint. As also illustrated in Fig. 3, it is calculated as

$$\Delta v_o = \Delta v_{C2} = \frac{I_o - I_L}{C_1 + C_2} DT_s + \frac{I_o - I_L}{C_2} D'T_s. \quad (12)$$

Since S-Hybrid converter merges SI and SC operations, output voltage ripple Δv_o depends on both C_1 and C_2. On the other hand, the effective voltage ripple of C_1 that contributes to switched-capacitor loss is determined by

$$\Delta v_{C1,eff} = -\frac{I_o - I_L}{C_1 + C_2} DT_s + \frac{I_L}{C_1} D'T_s. \quad (13)$$

Given a fixed resource with a fixed total capacitance, the sum of C_1 and C_2 is a constant. In this case, as seen in (12) and (13), partitioning more capacitance to C_2 can reduce the output voltage ripple but increase voltage ripple on C_1, which makes the voltage difference between v_{C1} and v_{C2} at the beginning of phase 1 increase and aggravates the switched-capacitor loss [6]. Furthermore, the excessive voltage surge on C_1 increases voltage stress on switch S_1 which would increase its switching loss and affect circuit reliability, e.g. transistor breakdown. To analyze the switched-capacitor loss variation with different operating conditions, total switched-capacitor loss can be derived as

$$P_C = \frac{1}{2}\frac{C_1 C_2}{(C_1 + C_2)}\left(\Delta v_{C1,eff} + \Delta v_o\right)^2 \frac{1}{T_s}. \quad (14)$$

Fig. 9 illustrates a graphical representation of voltage ripples

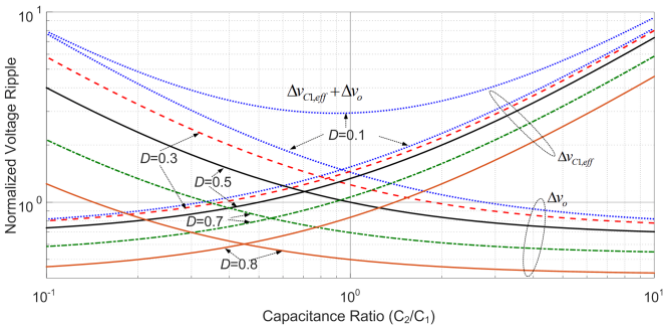


Fig. 9. Normalized capacitor voltage ripples as a function of capacitance ratio with different duty cycles.

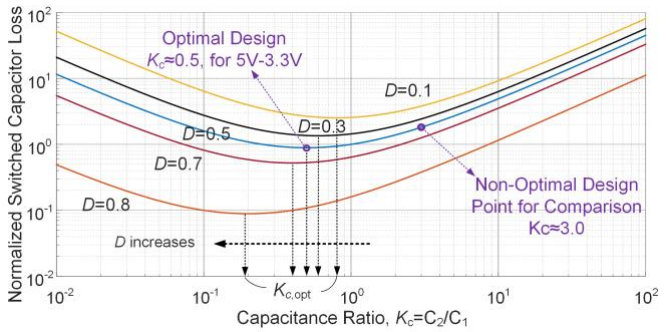


Fig. 10 Switched capacitor loss as a function of capacitance ratio with different duty cycles. Optimal capacitance ratio is found for minimum loss.

with different capacitor ratios and duty cycles with constant output current condition. In this figure, ripple voltages $\Delta v_{C1,eff}$ and Δv_o are normalized to the output voltage ripple at unity capacitance ratio and fixed duty cycle 0.5 to neutralize the impact of change in design parameters such as total capacitance or output load. This graphical analysis visualizes a design point when the worst voltage ripple occurs. Both voltage ripples increase as duty cycle D decreases, leaving larger interval (1—D)T_s, when two capacitor voltages deviate, and larger difference between I_L and I_o. To account for the worst case, minimum duty cycle D_{min} is chosen as a design condition. In addition, maximum load current $I_{o,max}$ is chosen as a reference design point. Once the design point is recognized, optimal capacitance ratio is identified using (14).

Fig. 10 displays P_C as a function of capacitance ratio at different duty cycles. In the same manner as voltage ripples, P_C changes in the opposite direction to duty cycle, and thus minimum duty cycle determines the most significant switched-capacitor loss. In this analysis, in addition, optimal capacitance ratios $K_{c,opt}$ can be identified to achieve minimum switched capactior loss. $K_{c,opt}$ is always smaller than 1, or $C_2<C_1$, for all duty cycles because during (1— D)T_s while C_1 needs to handle a charge proportional to I_L, C_2 only needs to handle (I_o – I_L), which is smaller than I_L for all M of interest. For example, with D = 0.5, $K_{c,opt}$ = 0.5. However, actual K_c may differ from $K_{c,opt}$ when other constraints, such as output voltage ripple and total capacitance, are enforced. More details are below.

In a certain system, final capacitance values can be determined based on operation range and system requirements including output voltage ripple specification and total capacitor size limit. A larger total available capacitance, i.e. more

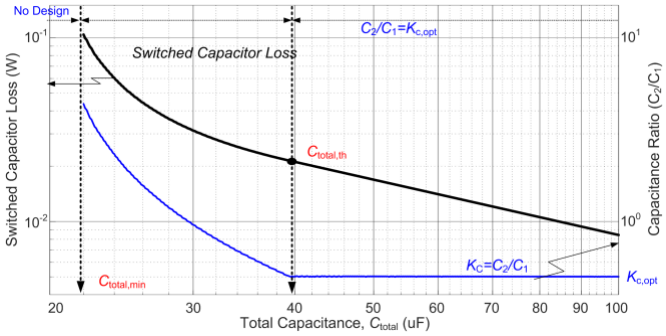


Fig. 11. Capacitor design optimization with different total capacitances. When $C_{total} < C_{total,th}$, the final design point of K_c stays off $K_{c,opt}$ to meet output voltage ripple constraint being forced to sacrifice switched capacitor loss.

resources, often leads to smaller converter loss, particularly for heavier loads [6]. Fig. 11 depicts the capacitor design for optimal switched-capacitor loss P_c with a limited total available capacitance C_{total} and maximum voltage ripple. In this analysis, D_{min}, switching frequency f_s, maximum output voltage ripple $\Delta v_{o,max}$, and $I_{o,max}$ are assumed to be 0.5, 2 MHz, 33 mV, and 3.9 A, respectively, with V_g=5 V and V_o=3.3 V. If C_{total} is not large enough, most capacitance should be assigned to C_2, or $C_2 \approx C_{total} = C_1 + C_2$, i.e. K_c remains larger than $K_{c,opt}$, to satisfy the required $\Delta v_{o,max}$. In this regime, $K_{c,opt}$ and P_C are sacrificed to meet $\Delta v_{o,max}$. When C_{total} is smaller than the required minimum total capacitance $C_{total,min}$, there is no possible design to meet all system requirements at the same switching frequency f_s. Using (13), $C_{total,min}$ can be derived as

$$C_{total,min} = \frac{(I_o - I_L)}{\Delta v_{o,max}} T_s. \quad (15)$$

When more capacitance is available, the amount of capacitance allotted to C_1 increases, i.e. K_c approaches $K_{c,opt}$. As a result, $\Delta v_{C1,eff}$ and thus P_C are dramatically decreased as illustrated in Fig. 11. The total capacitance threshold is defined when K_c becomes $K_{c,opt}$ is

$$C_{total,th} = \frac{(I_o - I_L)T_s}{\Delta V_{o,max}} \left(D + \frac{(1-D)(1+K_{c,opt})}{K_{c,opt}} \right). \quad (16)$$

Once the total capacitance reaches $C_{total,th}$, P_C can be minimized by optimally allocating capacitances in ratio of $K_{c,opt}$. After this point, P_C optimally scales with C_{total} at the fixed capacitance ratio $K_{c,opt}$.

Based on this analysis and considerations for the capacitor components, a converter prototype is designed to manage the switched-capacitor loss in Section V. Experimental data of a design variation with a non-optimal capacitor ratio K_c are also presented for comparison and further discussions.

B. Semiconductor Design

Semiconductor devices for S-Hybrid converter can be determined based on loss analysis and system requirements similar to capacitor design. Two key parameters considered for loss analysis are: on-state resistance and parasitic capacitances. With a chosen semiconductor process, the two parameters involve a trade-off where a larger switch has smaller on-state resistance, thus smaller conduction loss, but has larger switching loss due to larger parasitic capacitance, and vice versa. Therefore, switch design process needs careful optimization for minimum total loss.

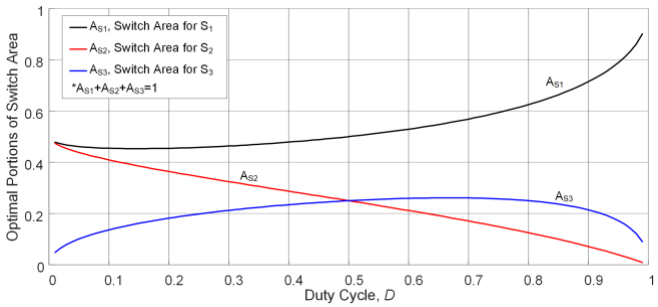


Fig. 12. Optimal switch die area portions as a function of duty cycle. With a given semiconductor die area or form factor, the die area ratios can be found.

Employing the average model of S-Hybrid converter, one can design the switches in three steps: 1) determine a design point, i.e. recognize operating conditions to optimize, 2) identify switch loss contribution based on the model 3) find optimal switches (in discrete implementations) or optimal switch sizes (in integrated circuit implementations) from a set of given switch types, e.g. TI MOS switches, to meet the target design. For a S-Hybrid converter design scenario accounting for a worst-case switch conduction loss, the condition for minimum duty cycle $D_{\min}$ would be the design point based on the analysis illustrated in Fig. 8. In another design scenario, the priority can be to achieve higher efficiency in a most frequently operated range of output voltage, load, or conversion ratio. Either design scenario leads to minimizing the output resistance given by (11) at a design point. For switch design, that is to find

$$min\left(\frac{R_{S1}}{D}+\frac{(D')^2R_{S2}}{D}+D'R_{S3}\right). \qquad (17)$$

Given a fixed total switch area (for implementation cost control) and thus a fixed total switch conductance, allocation of the three switches A_{Si} can be determined for different duty cycles as illustrated in Fig. 12. Note that $A_{S1}+A_{S2}+A_{S3}=1$ and A_{Si} is proportional to switch conductance G_{Si} and inversely proportional to switch resistance R_{Si}. As shown in Fig. 12, area portion A_{S1} of S_1 remains the largest because of its largest contribution to the output impedance as displayed in Fig. 8. Optimal area for S_2 is inversely proportional to D because as D increases, the accumulated charge to be balanced through S_2 decreases.

To finalize the switch design, total loss including conduction and switching losses would be considered. Since the trade-off between conduction and switching losses is similar with conventional converters, optimal design can be derived from the discussion above with a traditional design methodology [18].

C.Small Signal Model and Control

To design a controller for S-Hybrid converter regulation, its dynamic characteristics are analyzed, and discussion on the effect of input voltage and cable variations is provided. Since the sub-circuits of S-Hybrid converter are linear and can be expressed by state equations in each phase, state space averaging can be used to derive the converter transfer functions. Accounting for on-resistance of semiconductor switches and cable resistance, the control-to-output voltage transfer function can be derived as

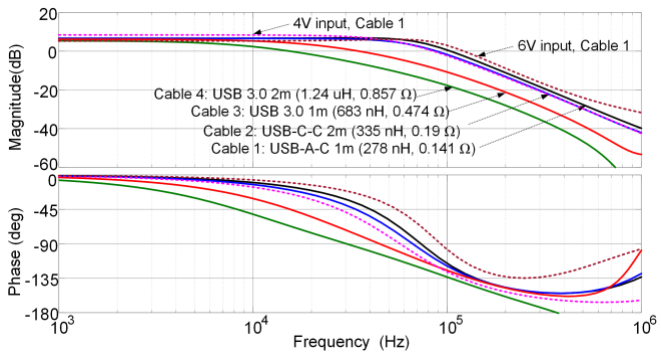


Fig. 13. Control-to-output voltage transfer functions with different USB cables and input voltages at 3.3V/1A output condition.

$$G_{vd}=I_LR_o\frac{\left(1+\frac{s}{k_{vd}}+\frac{s^2}{\omega_{0,vd}^2}\right)\left(1+\frac{s}{\omega_{esr}}\right)}{\left(1+\frac{s}{\omega_0Q_0}+\frac{s^2}{\omega_0^2}\right)(1+s/\omega_p)} \qquad (18)$$

where $\omega_0=\frac{1}{\sqrt{C_eL_e}}$, $Q_0=\frac{(2-D)^2}{R_L}\sqrt{\frac{L_e}{C_e}}$, $\omega_p=\frac{DG_sC_e}{C_1C_2}$, $L_e=\frac{L}{(2-D)^2}$, $C_e=C_1+C_2$, $\omega_{0,vd}=\frac{1}{\sqrt{C_1L_e}}\sqrt{\frac{D^2I_LR_oG_s}{D'}}$, $\omega_{esr}=\frac{1}{C_2R_{c2}}$, $G_s=\frac{1}{(R_{s1}+R_{s2})}$, and $k_{vd}=\frac{DV_{C2}G_s(2-D)}{\left[I_L(2-D)R_oC_1G_s(R_{s2}+D'R_{s1})+\frac{D'}{D}I_LC_1R_L-DLG_sI_L\right]}$. The detailed derivation of the converter transfer function can be found in [19].

Since the S-Hybrid converter architecture uses a cable parasitic inductance, considering inductance variations is important in the controller design. Fig. 13 shows the open loop control-to-output voltage transfer functions with four different USB cables with different inductance and ESR. Since the cable inductance determines the location of the system's double pole and cable resistance defines the system damping factor, and the type and location of zeros as expressed in (18) [19], it is observed that the mid-to-high frequency response heavily depends on the cable parameters, implying the need for additional efforts in a range of usable cables and controller designs. Fig. 13 also illustrates the effect of input voltage variations, which would be considered in the design.

Considering the effects of input voltage and cable parameter variations, a two-poles two-zeros voltage compensator (type III) is used for stability and transient analyses. The compensator is designed to have a 243-kHz cut-off frequency and 54.5° phase margin for a 1 m USB cable (Cable 1: 278 nH, 0.141 Ω) at 3.3V/3.9A condition (nominal operation point), and maintain stable operations for all other operating conditions.

Assuming the same compensator, it is of interest to analyze the converter dynamic characteristics with different input voltages and cables. The loop gains of the converter at a fixed 3.3V/1A output with two different input voltages and four different cables are presented on Fig. 14. As the cable inductance increases (from Cable 1 to 4), the cut-off frequency decreases as the system double pole frequency decreases. In addition, since the cables with higher inductance tend to have higher resistance resulting in low Q, split system poles affect the phase margin. To the contrary, small cable inductance will

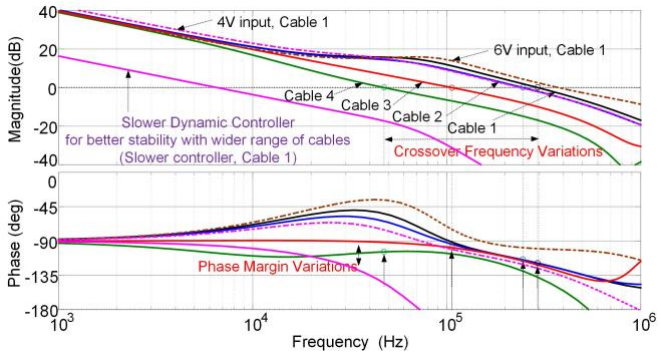


Fig. 14. Control loop gains of a type III compensator with different cables and input voltages at 3.3V/1A output condition.

push cut-off frequency higher and eventually de-stabilize the system by approaching Nyquist limit or by insufficient phase margin. On the other hand, the effect of input voltage changes is relatively small as shown in Fig. 14.

In conclusion, this analysis indicates that the converter system can retain stability with different USB cables using a proper controller design. The converter dynamics follows the traditional trade-off of response speed and stability. For example, one can have fast response with the cost of varying dynamic performance, or achieve stability across a larger range of input cables by designing the controller with an intentional low cut-off frequency and thus slow response. To illustrate this point, another loop gain curve is added to Fig. 14 describing the use of another Type-I compensator to achieve 83° phase margin at a lower cut-off frequency, 6.07-kHz, for the same Cable 1. To guarantee the system operation, a certain range of cables may be defined along with the controller design. Another potential solution to allow a wider range of cables can be adding a small inductor designated in series with the cable to limit the minimum input inductance as well as the cut-off frequency.

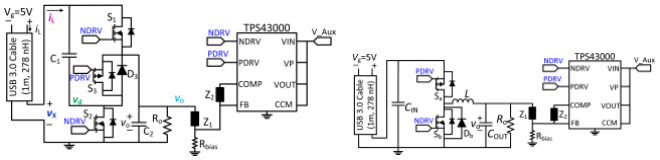
V. Experimental Verification

In order to validate the converter architecture utilizing cable parasitics for power conversion, a 5-V to 3.3-3.8-V 15-W S-Hybrid converter prototype and its Buck converter counterpart are implemented. The prototype uses a 1 m input USB cable that has 278 nH parasitic inductance and employs no dedicated inductor, as illustrated in Fig. 15. Its Buck counterpart is equipped with a 0.9 µH chip inductor in a 2.5 mm x 2.0 mm x 1.0 mm package. Capacitances C_1 and C_2 for prototype are determined based on the analysis in Section IV; in this design example C_{total}=39.8 µF and $K_{c,opt}$≈0.5. For a fair comparison, both converters employ the same MOSFETs and controller. The same controller is used to drive the switches in the S-Hybrid and Buck converters. Circuit components and parameters for hardware verification are detailed in Table III.

The experimental setup and the converter prototype are shown in Fig. 16 where the 1 m USB 3.0 cable is used as inductor for the prototype. The experimental waveforms at full load and 3.3 V output shown in Fig. 17 verify the converter operation described in Section II.B. The duty cycle of approximately 70%, increased from the ideal 50%, seen in this

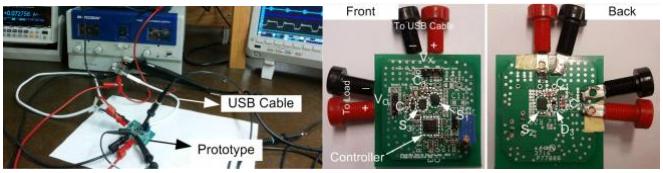
TABLE III. Circuit Component and Parameters.

Item	Design Selection
Controller	TPS43000, Texas Instruments
f_s	2 MHz
Input Cable	USB-A to C, 278 nH, DCR: 0.141 Ω, 1m, Belkin
C_1	26.6 µF, 2 x 10 µF + 2 x 3.3 µF)
C_2	13.2 µF, 1 x 10 µF + 1 x 3.3 µF
Capacitor	10 µF: X7R, 1206, ESR: 6.5 mΩ at 2 MHz, TDK
Elements	3.3 µF: X5R, 0603, ESR: 4.8 mΩ at 2 MHz, TDK
C_{IN}, C_{OUT}	20 µF, X5R, 1.6 mm x 0.8 mm, Murata
L for buck	0.9 µH, DCR: 0.050 Ω, 2.5 mm x 2.0mm x 1.0 mm
S_1, S_2, S_b	CSD16327Q3, NMOS, SON 3.3 mm x 3.3 mm, TI
S_3, S_a	CSD25404Q3, PMOS, SON 3.3 mm x 3.3 mm, TI
D_3, D_b	BAT60A, 2.5 mm x 1.25 mm, Infineon



(a) (b)

Fig. 15. Converter circuit implementations: (a) S-Hybrid, (b) Buck.



(a) (b)

Fig. 16. Experimental verification: (a) converter setup using a USB cable as inductor, (b) converter prototype PCB front and back.

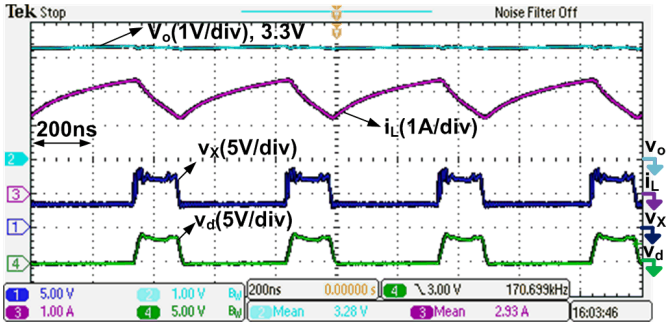


Fig. 17. Measured waveforms of prototype at 5-V to 3.3-V/3.9-A condition.

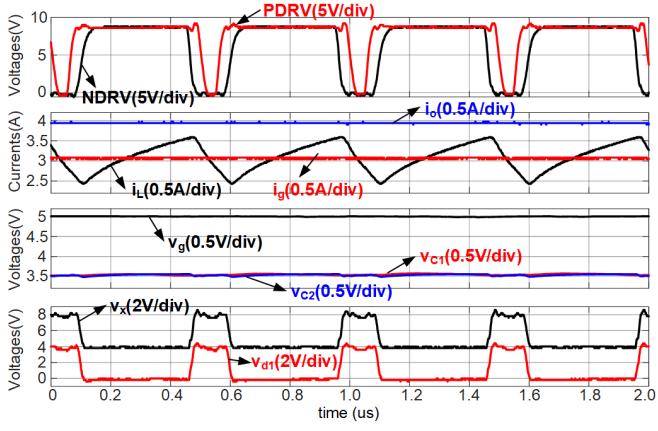


Fig. 18. Measured waveforms of prototype at 5-V to 3.5-V/3.9-A condition.

experiment is the result of practical resistive components, in good agreement with analysis in Section III as also illustrated

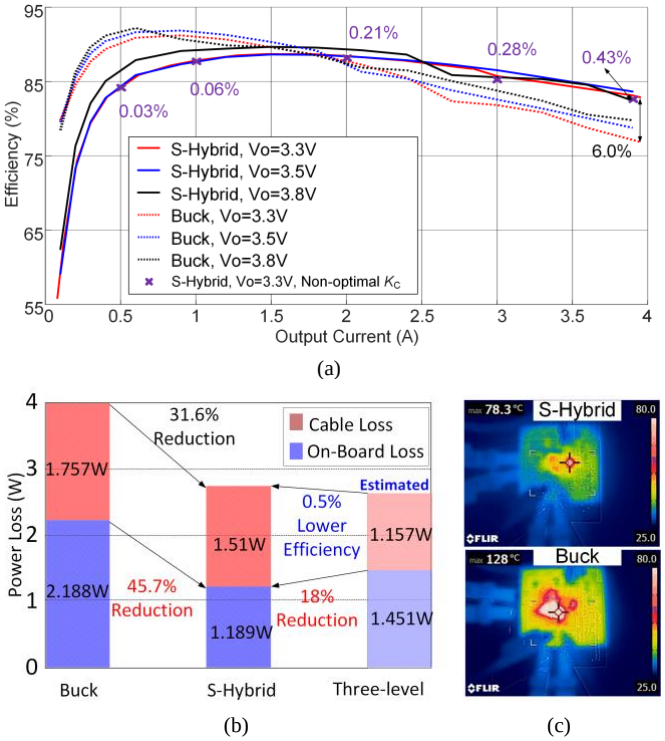


FIg. 19. Measured efficiency comparison: (a) system efficiency comparison, (b) loss breakdown, (c) thermal image comparison in steady state operation.

in Fig. 6. Figure 18 shows additional measured waveforms using a 1 GHz oscilloscope, including the gate-drive signals NDRV and PDRV from the controller, output current i_o, input current i_g (before the input capacitor), supply voltage v_g, capacitor voltages v_{C1} and v_{C2}, and the two switching nodes v_X and v_{d1}. The converter operation agrees with the analysis. With the controller, it regulates the output voltage at 3.5 V.

Efficiencies of the S-Hybrid and Buck converters are measured and shown in Fig. 19. S-Hybrid converter archives better efficiency in mid to full loads, the most critical load range for heat management. It achieves up to 6.0% efficiency improvement, equivalent to 31.6% loss reduction, at rated load owing to zero dedicated inductor and lower inductor current ripple loss. Note that the calculations shown in FIg. 19(b) includes cable loss for Buck converter to represent a complete end-to-end efficiency from the input DC source, e.g. AC-DC adapter output, to the battery.

More importantly, S-Hybrid converter experimentally exhibits a superior on-board thermal reduction advantage, potentially enabling further miniaturization and integration in a future design. Counting only power components on circuit board, the prototype S-Hybrid converter has 45.7% less on-board loss compared with the Buck converter, as shown in FIg. 19(b). Estimated performance of a three-level Buck converter is also added in this comparison, assuming it uses the same MOSFET devices and an output inductor with 3X lower inductance and 3X better ESR (L=0.3 uH, 18 mΩ) thanks to its superior inductor current ripple as discussed in Section III.A and Fig. 4. Although the three-level converter achieves 0.5% better overall efficiency, S-Hybrid dissipates 18% less on-board loss because of on-board inductor removal. Thermal image captures at the same 3.3 V/3.9 A output steady state operation by a FLIR E6 in FIg. 19(c) agree with the efficiency and loss characterization proving significant potential benefit of S-Hybrid architecture in thermal management. This significant on-board loss reduction and heat mitigation proves the new architecture is a promising candidate for mobile and wide range of other applications where system thermal is already at its limit.

To evaluate the effect of capacitance allocation on converter loss discussed in Section IV.A, the same prototype converter with a non-optimal capacitance allocation is tested for efficiency measurement. From the same total capacitance of ~40 µF, ~10 µF is allocated to C_1 and ~30 µF to C_2, yielding K_c≈3 different from the optimal value K_c=0.5. The same TDK 3.3 µF and 10 µF capacitors are used for this converter configuration. The efficiency data is overlaid on FIg. 19(a) for comparison. As expected, the converter's efficiency is lowered in the entire load range but more significant at the rated load condition, 3.3V/3.9A, with 0.43% efficiency decrease. The impact much less significant at light loads because the contribution of the switched-capacitor loss to efficiency reduces, similar to the conduction loss. Since loss management at heavy load dictates the converter's capacity given a fixed thermal limit, it is important to have an optimal capacitance allocation for optimal S-Hybrid converter operations.

Table IV compares the converter prototype in this work with commercial Buck converters. It achieves high Q factor [20] even with the smallest passive component volume thanks to the dedicated inductor elimination, while Buck converters need bulky inductors, i.e. large passive volume, for high Q factor or have more loss for a more compact size. Conclusion

This paper presents an S-Hybrid step-down architecture that employs parasitic inductance of a power delivery USB cable to

TABLE IV. COMPARISON WITH COMMERCIAL BUCK TYPE CONVERTERS.

	S-Hybrid (This work)	Buck (this paper)	LMR10530X	TPS51313	PMP4771	TPS82085
Topology	S-Hybrid	Buck	Buck	Buck	Buck	Buck
Input	5V	5V	5V	5V	5V	5V
Output	3.3V/3.9A	3.3V/3.9A	3.3V/3A	3.3V/3A	3.3V/3A	3.3V/3A
Switches	3	2	2	2	2	2
Capacitors	2 (C1 & C2)			2 (input & output capacitors)		
Inductor (ind., ESR, vol.)	None	0.9uH, 50m, 2.5x2x1mm^3	1.2uH, 28m, 5.2x5x2.2mm^3	0.56uH, 18.7m 3x3x1.2mm^3	10uH, 25m, 10x9.7x4.5mm^3	0.47uH, N/A N/A
Passive vol.	5.76	9.608	73.584	17.05	472.46	N/A
Frequency (f_{sw})	2MHz	2MHz	1.5MHz	1MHz	550kHz	2.4MHz
Q factor=$P_{out}/P_{loss,on\text{-}board}$	10.82	5.88	8.74	3.17	19.41	11.50

feature zero dedicated inductor and less reliance on magnetic component - all are significantly advantageous for better future integration. The hybrid converter circuit operation, its steady-state analysis, and key benefits are discussed using converter average model. This paper further provides additional analysis and optimization for capacitors and switches as design guidelines in practical implementations. Measured results from a 15-W prototype using USB cable and no magnetic component confirm the architecture functionality and analyses. The prototype converter achieves superior performance at mid to high loads compared with a conventional Buck converter counterpart and reduces the on-board loss and thus heat dissipation by about two times. Given the achievements with relatively simple implementations, the results illustrate that S-Hybrid architecture is indeed a promising candidate to realize future smart power cables that can provide both power transmission and power conversion in a wide range of applications.

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